

FIGURE 1
(Prior Art)

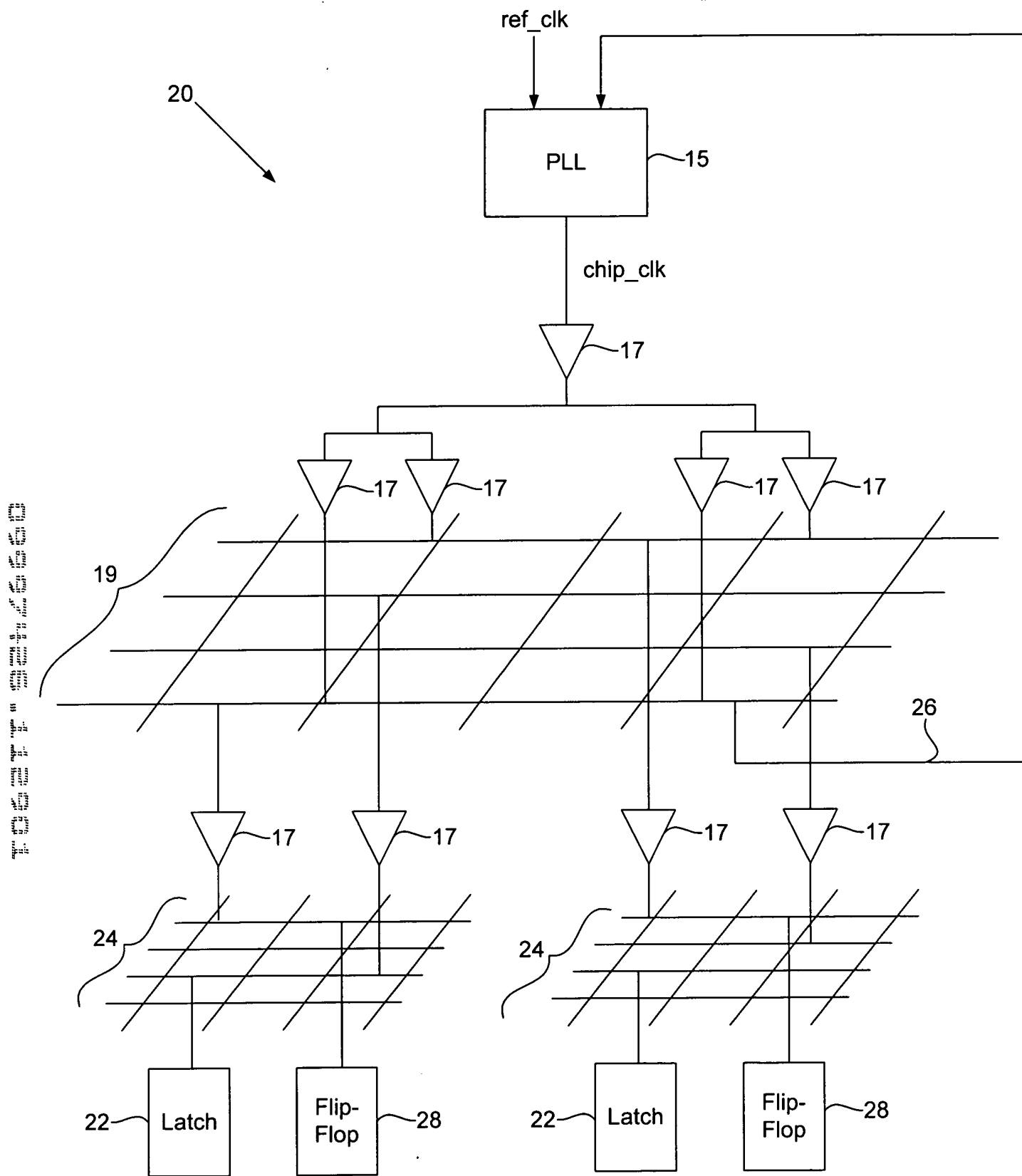


FIGURE 2
(Prior Art)

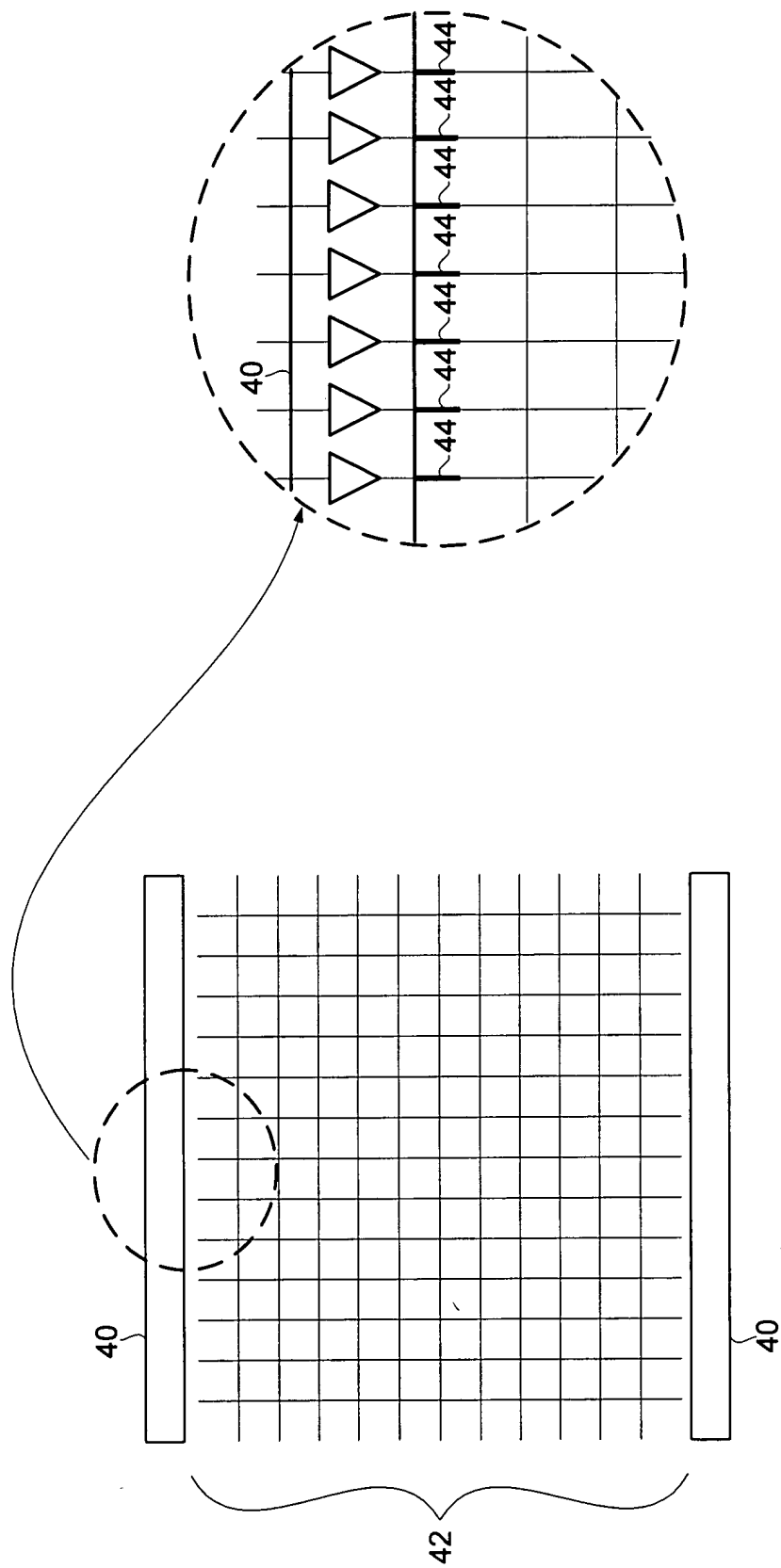


FIGURE 3a
(Prior Art)

FIGURE 3b
(Prior Art)

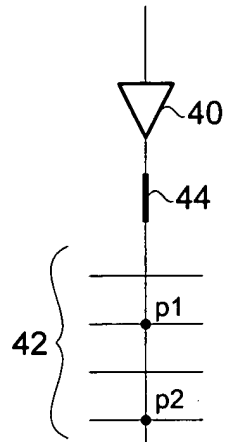


FIGURE 3c
(Prior Art)

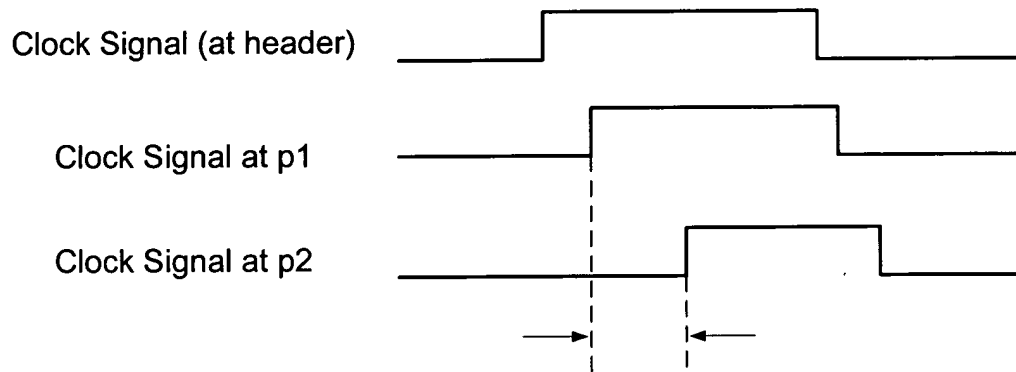


FIGURE 3d
(Prior Art)

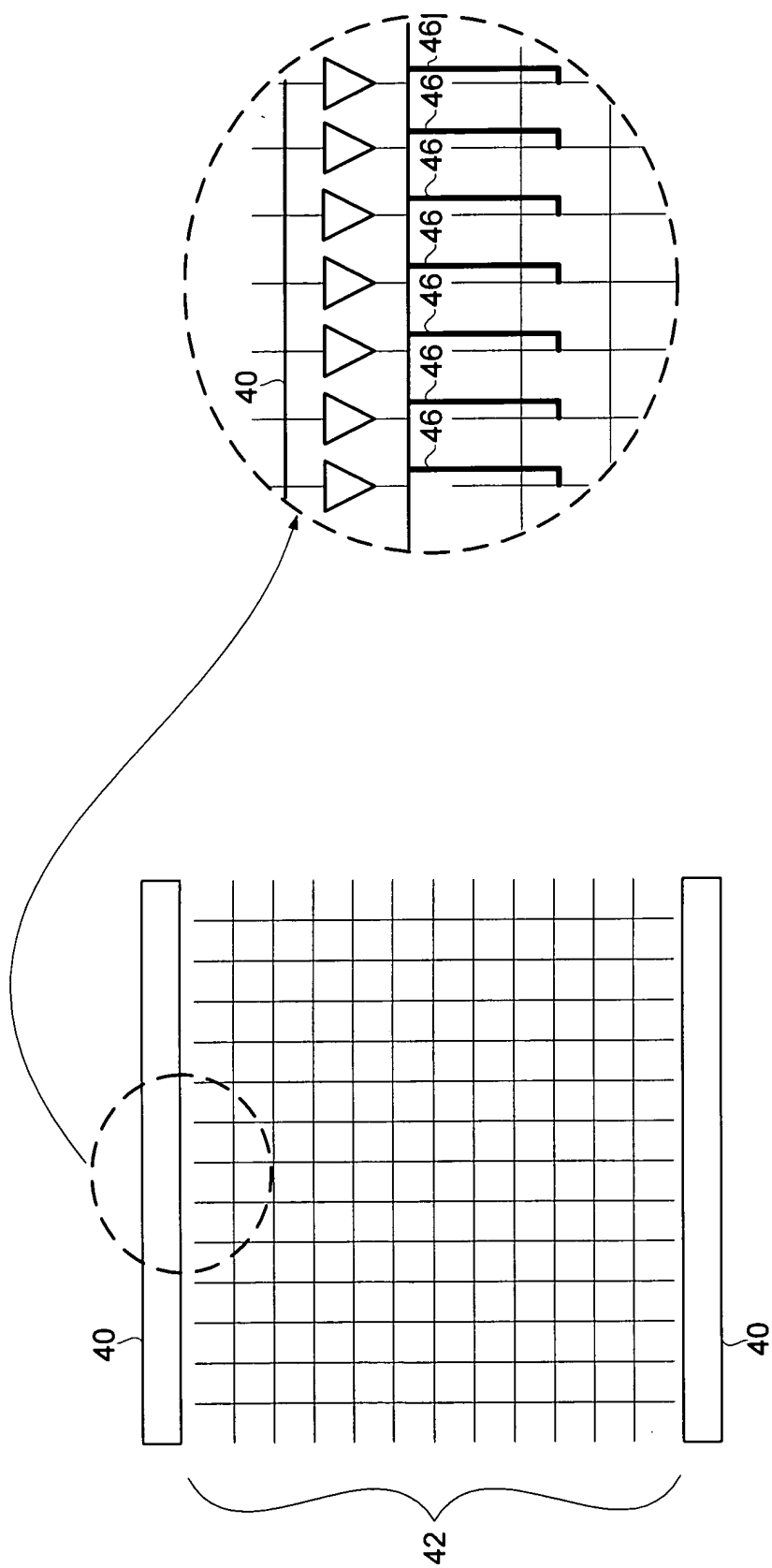


FIGURE 4a

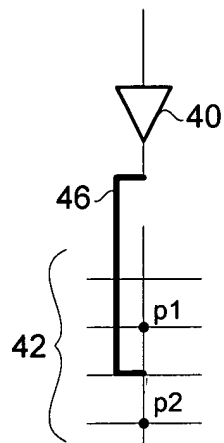


FIGURE 4b

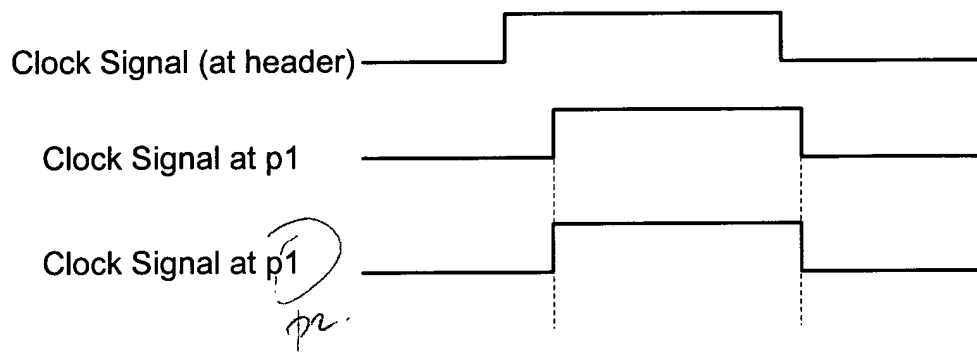


FIGURE 4c

FIG. 5 is a schematic diagram of a circuit 40, which includes a plurality of input lines 42, a plurality of output lines 44, and a plurality of control lines 46. The circuit 40 is configured to receive a signal on one of the input lines 42 and output a signal on one of the output lines 44 in response to a control signal on one of the control lines 46.

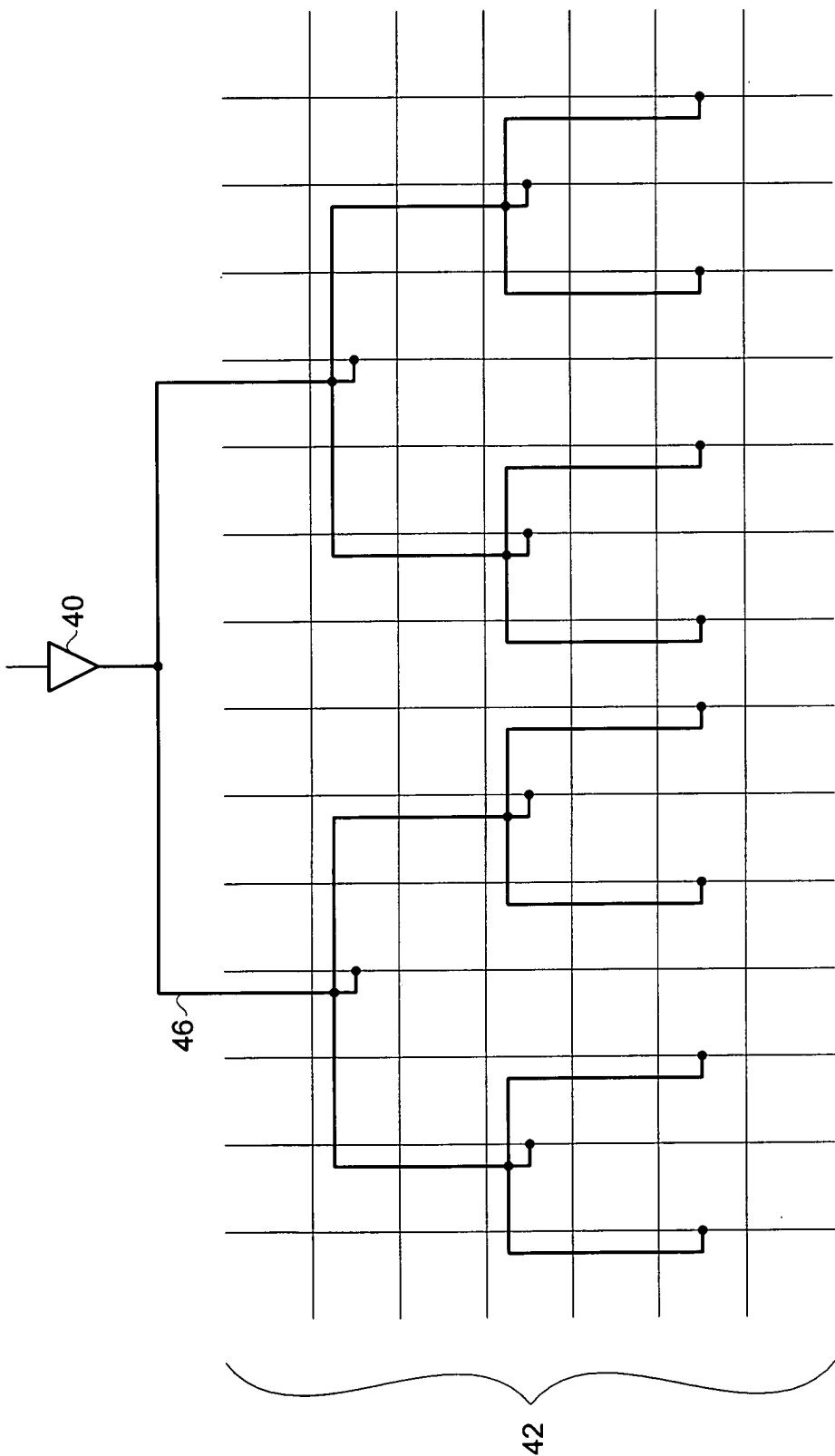


FIGURE 5